Amendments to the Claims

The listing of claims presented below will replace all prior versions, and listings, of claims in the application.

Listing of claims:

1-13. (cancelled)

14. (previously presented) A synchronous memory device for synchronization of an external input clock with an internal input clock comprising:

a delay locked loop (DLL) having a clock divider comprising a plurality of clock signal dividers connected in series,

a power down controller determining a power down condition based at least on a predetermined state of a clock enable signal that controls whether the memory device receives the external input clock and that is inputted to the DLL,

wherein the clock divider outputs a first clock signal being one of the output signals of the clock signal dividers excluding the last clock signal divider of the series when the synchronous memory device is in the a non-power down condition,

wherein the clock divider outputs a second clock signal being an output signal of the last clock signal divider of the series when the synchronous memory device is in the power down condition, and

wherein a frequency of the first clock signal is higher than that of the second clock signal.

15. (previously presented) The synchronous memory device of claim 14, wherein the frequency of the first clock signal is 2M when the frequency of the second clock signal is M.